

WHAT IS CLAIMED IS:

1. A logic circuit comprising an arithmetic logic unit (ALU) performing a logical operation or an arithmetical operation, and a control circuit controlling said ALU, wherein said control circuit receives, as an input, a program including  
5 a plurality of instructions defining the type of an operation to be executed on an ALU and information showing a dependency between said plurality of instructions and controls said ALU according to said program.
2. The logic circuit according to claim 1, wherein said control circuit decides an execution order of said plurality of instructions according to said information showing a dependency to supply the executable one of said  
5 plurality of instructions to said ALU.
3. The logic circuit according to claim 2, wherein said information showing a dependency is information on an antecedent instruction which must have been executed in order to execute the corresponding one of said plurality  
5 of instructions,  
said control circuit decides whether said antecedent instruction is executed.
4. The logic circuit according to claim 2, wherein  
said logic circuit has a plurality of said ALUs,  
said control circuit outputs the executable ones of said plurality of instructions to said ALUs in parallel.
5. The logic circuit according to claim 1, wherein  
said logic circuit is a re-configurable processor,  
said ALUs include a plurality types of operations and

are arrayed,

5           said program includes definition of data used as an  
input and output of an operation, specification of said  
operation type to said ALU, specification of a connection  
state of wiring between said arrayed ALUs, and information  
on input data necessary for the corresponding one of said  
10 arrayed ALUs to perform an operation,

          said control circuit controls the connection state  
of wiring between said arrayed ALUs according to said  
inputted program to decide whether said corresponding ALU  
is executable.

6. A program which allows a logic circuit having an ALU  
performing a logical operation or an arithmetical operation  
and a control circuit controlling the ALU to execute a  
desired operation by giving an instruction to said ALU via  
5 said control circuit, comprising an instruction defining  
the type of an operation to be executed on said ALU and  
instructions defining the types of operations to be  
executed on a plurality of ALUs, wherein an execution order  
dependency existing in said instruction or between said  
10 instructions is described.

7. The program according to claim 6, wherein said plurality  
of instructions or instruction blocks having said  
instructions are defined, and an execution order dependency  
between said instruction blocks is described.

8. The program according to claim 6 or 7, which describes:  
          an execution order dependency existing in said  
instruction or between said instructions or said

instruction blocks;

5           operations having said instruction, said  
instructions or said instruction blocks;

          data of an input or output of said instruction, said  
instructions, or said instruction blocks;

          a relation between said operations and data necessary  
10   for executing said operations; and

          a relation between said operations and data generated  
by said operations.

9. The program according to claim 6, wherein in order to  
start an operation or operations defined by said  
instruction or said instructions, an antecedent  
instruction which must have been executed is described.

10. The program according to any one of claims 6 to 9, which  
is intended for a re-configurable processor having said  
arrayed ALUs and controlling operation by specification of  
an operation type to said ALU and specification of  
5   connection between said ALUs.

11. The program according to claim 10, wherein an  
instruction block defined by specifying, to one or more ALUs,  
definition of data used as an input and output of an  
operation, specification of an operation type to said ALU,  
5   and specification of wiring between said ALUs, has  
information on input data necessary for performing an  
operation.